Form PTO-1449				Complete if Known	
				Application No.:	not yet assigned
INFORMATION DISCLOSURE STATEMENT				Filing Date:	
				First Named Inventor:	Richard FOSS
				Group Art Unit:	
				Examiner Name:	
Sheet	1	of	2	Attorney Docket No.:	PAT 819-2

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document No.	Date of Publication mm-dd-yyyy	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
GL		4,942,575	07-17-1990	Earnshaw et al.	
		4,901,320	02-13-1990	Sawada et al.	
		6,185,718	02-06-2001	Dell et al.	
		6,233,717	05-15-2001	Choi	
		6,353,910	03-05-2002	Carnevale et al.	
		5,127,014	06-30-1992	Raynham	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Patent Document No.	Date of Publication mm-dd-yyyy	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T √	Check if English Translation is attached

OTHER DOCUMENTS

GL		P. Mazumder, "An On-Chip ECC Circuit for Correcting Soft Errors in DRAM's with Trench Capicitors", IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, pages 1623-1633.
		ISSCC 83, Friday, February 25, 1983, Imperial Ballroom A, 11:45am., Session XVI: 256K DRAMs, "FAM 16,6: Submicron VLSI Memory Circuits", T. Mano, J. Yamada, J. Inoue, S. Nakajima, 1983 IEEE International Solid-State Circuits Conference
		ISSCC 84, Wednesday, February 22, 1984, Continental Ballrooms 6-9, 4:30pm, Session VIII A: 256K 1Mb DRAMs I, "WPM 8A.5: A Submicron VLSI Memory with a 4b-at-a-Time Built-in ECC Circuit", J. Yamada, T. Mano, J. Inoue, S. Nakajima, T. Matsuda, 1984 IEEE International Solid-State Circuits Conference

Examiner Signature:	Date Considered:
/Guy Lamarre/ (07/17/2006)	

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GL		4,183,463	01-15-1980	Kemmetmueller	
		4,679,196	07-07-1987	Tsujimoto	
		6,125,466	09-26-2000	Close et al.	
		5,134,616	07-28-1992	Barth, Jr., et al.	
		4,688,219	08-18-1987	Takemae	
		4,768,193	08-30-1988	Takemae	
		4,456,980	06-26-1984	Yamada et al.	
		4,747,080	05-24-1988	Yamada et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Patent Document No.	Date of Publication mm-dd-yyyy	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T √	Check if English Translation is attached

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